Flexible Charge Balanced Stimulator With 5.6 fC Accuracy for 140 nC Injections

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***Abstract*—Electrical stimulations of neuronal structures must ensure net injected charges to be *zero* for biological safety and voltage compliance reasons. We present a novel architecture of general purpose biphasic constant current stimulator that exhibits less than 5.6 fC error while injecting 140 nC charges using 1.4 mA currents. The floating current sources and conveyor switch based system can operate in monopolar or bipolar modes. Anodic-first or cathodic-first pulses with optional inter-phase delays have been demonstrated with *zero* quiescent current requirements at the analog front-end. The architecture eliminates blocking capacitors, electrode shorting and complex feedbacks. Bench-top and *in-vivo* measurement results have been presented with emulated electrode impedances (resistor-capacitor network), Ag-AgCl electrodes in saline and *in-vivo* (acute) peripheral nerve stimulations in anesthetized rats.**

***Index Terms*—Charge balancing, electrical stimulation, floating current source, muscle evoked potentials (MEP).**

I. Introduction

ELECTRICAL stimulation is a widely adopted method for therapeutic interventions and functional restorations of neuronal systems. Stimulation of peripheral nerves [1], deep brain tissues [2], cochlea [3] and retinal neurons [4], [5] are common examples. The role of electronic stimulators and electrodes are paramount in such applications. Significant design challenges remain to be met in order to enhance safety and reliability.

Injected charges are mainly responsible for excitation of neural structures [6]. However, net charge injection must be *zero* for biological safety reasons [7]. *Non-zero* charge injection generates DC offset voltages at the electrode-electrolyte interface and within neural tissues. The corresponding electric field strengths can rise beyond tolerable limits and cause tissue inflammation and permanent damage [8]. High speed stimulation can severely intensify this problem. Additionally, inadequate charge balancing induces pH shift in biological electrolytes [9], which leads to dissolution of the electrode surface due to electrolysis [10]. Dissolution of electrode material introduces toxic substances into the biological environment [8]. Finally, overtime charge accumulation can lead to increased electrode impedances, which adversely affects voltage compliance during stimulations and noise in recordings.

A variety of passive and active charge balancing techniques have been reported in literature. Biphasic constant current stimulations are generally used for charge balancing purposes [5], [11]–[15]. These are preferred over constant voltage methods due to the ability of controlling injected charges irrespective of interface and biological impedances [16]. Successive constant currents with equal magnitudes (I) and opposite polarity are applied to biological samples with identical phase durations (t), for total injected charge to be *zero*. Practically, current sourcing (positive) and sinking (negative) paths are separate, which results in mismatch and charge imbalance. Commonly used 1 mA stimulations [17], [5], [18], [14], [15], [19] with mismatch of 100 nA or more can greatly accelerate neural damages [8]. Critical compensation is thus required to reduce current or charge errors below 0.001% [20]. In fact, the specified industry limit on current mismatch in cochlear implants is 25 nA [21].

Charge balancing is passively improved by connecting a large DC blocking capacitor (several hundred *nano-Farads*) in series to stimulator drivers [11], [22]. Smaller blocking capacitors (eg. 100 pF) and multiple stimulation sources are applicable at higher stimulation rates on the order of 10 MHz [12], but at the expense of increased noise and power. These capacitors must be discharged regularly to nullify integrated DC voltages [10]. Highly capacitive and large electrodes can reduce the need of blocking capacitors to some extent [23].

Shorting of electrodes is helpful to neutralize post-stimulation errors [19], [24]–[27]. Effectiveness of shorting is limited by the time constants of the electrodes' discharging path, initially stored charges and stimulation parameters (injected charges and rate). Shorting results in unidirectional discharging currents [28], which may cause unwanted neural response to neighboring sites [29]. This technique also introduces unbalanced charge injection to the biological samples, although useful to neutralize residual voltages from the electrodes' interfacial capacitances.

Recently, active charge balancing techniques have gained popularity. Charge balancing through dynamic current matching and electrode shorting has been demonstrated. Current errors down to 1 nA and charge errors down to 6 pC have been reported using these techniques [29], [30]. Alternate

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methods to reduce the effects of stimulation mismatches adopt measurement of charge error and apply necessary compensation. Errors are estimated through post-stimulation electrode voltages [31] or using charge-metering through switch-capacitor networks [6]. Compensation is applied though suitable current offsets [10], [31] or dumping small charge packets to achieve charge errors down to 0.2% [6]. Feedback loop accuracies and stabilities are always critical in these methods.

Charge balanced stimulators with simpler design, higher accuracy and reliability can greatly benefit neuro-stimulation applications. An obvious need for better charge balancing stimulator exists where high speed and precise operations are important. We present an improved stimulator using floating current sources and steering diodes to achieve better than 5.6 fC accuracy while delivering 140 nC per phases. Programmable stimulation currents up to 1.4 mA have been shown possible with less than a 27 pA mismatch between the positive and negative phases. The analog front-end of the stimulator consumes *zero* quiescent current. 1.6 μW is consumed by the low overhead controller. The system can operate up to 35 KHz in monopolar or bipolar modes, and can generate anodic-first or cathodic-first biphasic pulses, with or without inter-phase delays. The proposed architecture eliminates the need for blocking capacitors, shorting of electrodes and critical feedbacks. Electrical characterization results have been presented with equivalent electrode impedances and Ag-AgCl electrode in phosphate buffered saline solution. *In-vivo* stimulations of the sciatic nerve with simultaneous evoked potential recordings have been performed in anesthetized rats.

The organization of the paper is as follows. Section II describes the architecture and design aspects. Section III and IV discusses bench-top and *in-vivo* experiments and results. Finally, Section V summarizes the features and highlights the improvements over existing stimulators.

II. System Architecture

Electrical stimulation results in multiple current paths in biological structures containing complex electrical networks. It is therefore non-trivial to design a perfectly charge balanced stimulator. Accurate current and phase time matching are essential to ensure quality charge balancing.

A. Principle of Operation

The principle of operation of the proposed charge balancing stimulator is to use an active constant current device for both the source (positive, $+I$) and the sink (negative, $-I$) phases, as shown in Fig. 1. Hence, the current matching is inherently accurate. The direction of load current is controlled through the relative orientation of the current sourcing/ sinking device and the load, with respect to the supply voltage rails. Identical phase timings are required in addition to achieve close to *zero* net charge injection.

B. Stimulator Architecture

Fig. 2 illustrates the schematic of the charge balanced stimulator. The analog front-end consists of unidirectional constant current sources and a full bridge steering or conveyor network

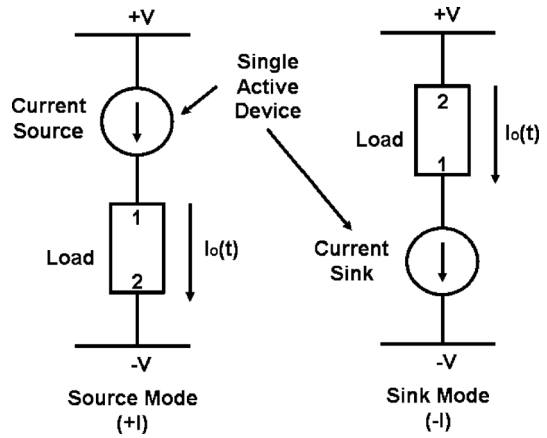

Fig. 1. Single current stabilizing device can actively operate in sink and source modes for charge balanced biphasic stimulations.

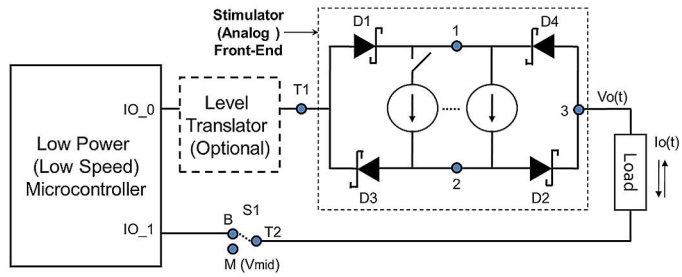

Fig. 2. Schematic of the charge balanced stimulator.

using Schottky diodes. A low speed microcontroller (e.g., $<$ 200 KHz) generates voltage controlled timing signals through its output mode IO (input-output) terminals, while saving dynamic power consumption. An optional level translator helps increase the load voltage range. The switch, S1, configures the stimulation mode as either bipolar (*B*) or monopolar (*M*). Switch position *M* is held at a fixed voltage, V_{mid}, and acts as reference in monopolar mode.

Magnitudes of output current are adjustable through hardware connections of discrete sources in parallel. Whereas, relative voltages at terminals *T1* and *T2* determine the direction of output current. Positive load currents are conveyed through the nodes *T1*, *1*, *2*, *3* and *T2*, while diode *D1* and *D2* are forward biased. Negative load currents take the path through the nodes *T2*, *3*, *1*, *2* and *T1*, while *D3* and *D4* are forward biased only. It is important to note that irrespective of the directions of load current the constant current sources conduct uni-directionally.

A floating constant current source is an appropriate choice in our architecture, because it can operate in both source and sink modes. Floating current sources are driven through load currents and thus have added advantage of reduced overhead. These units require *zero* quiescent or extra current due to the absence of dedicated power terminals. A minimum shunt voltage drop of 1.2 V is required to operate its internal biasing network and folded cascode structure [32]. Maximum output current is limited by the input voltage supply, current carrying capability of the diodes and the load impedance.

Schottky diode based current steering network ensures reduced circuit overhead, fast transitions and low *ON* state

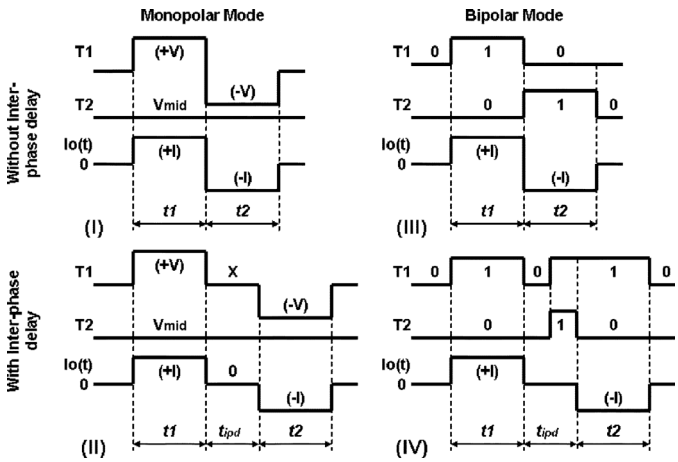

Fig. 3. Timing diagrams for a variety of operating (stimulation) modes.

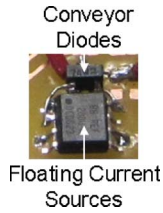

Fig. 4. Printed circuit implementation of the stimulator front-end.

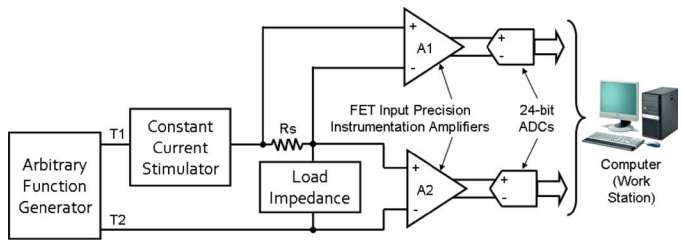

Fig. 5. Bench top characterization set-up for high-resolution measurements.

voltage drops. Faster switching improves dynamic performance, whereas, low *on-state* drop is advantageous for enhanced voltage compliance at the load. Steering action is dependent on relative voltages at *T1* and *T2*. Additional switch controls and feed-through noise have been avoided to ensure precise charge balancing.

C. Modes of Operation

The two-terminal stimulator can operate in monopolar and bipolar modes. The modes have been invoked by means of switch position (S1) and voltages at *T1* and *T2*. Hardware modification and extra power consumption are not required at the analog front-end to switch between the modes. The performance of charge balancing must be independent of the modes as similar voltage transitions are only required during stimulations. Fig. 3 represents the timing diagrams during various modes and sub-modes of operation.

1) Monopolar Mode: Monopolar stimulation is a convenient choice for multielectrode based applications with fixed reference, and particularly amenable to large area stimulations [33].The terminal *T2* needs to connect to position *M*, which acts as an analog reference (V_{mid}), for the proposed stimulator to act in monopolar mode. *T1* is driven to $+V$ and -*V* during positive and negative stimulation phases, respectively. The signals at *T1* are controlled digitally.

Theoretically, monopolar mode offers a maximum load voltage range of $+V$-$(-V)$-$2V_{drop}$, where, $+V$ and $-V$ are the dual supply voltages and V_{drop} is the combined voltage drop across the floating current source and the forward biased diodes. Assuming the supply voltage is ± 5 V and V_{drop} is 2 V, the load voltage range has been ± 3 V in monopolar mode.

2) Biopolar Mode: Bipolar mode is most useful for localized or single site stimulations [33]. Additionally, a single supply voltage along with digital control signals are sufficient to operate in this mode. Logic '*1*' ($+V$) in terminal *T1* and logic '*0*' (0 V) in terminal *T2* (S1 at position *B*) activates the positive load current. Logic '*0*' in terminal *T1* and logic '*1*' in terminal *T2* are required for the negative load current.

Although the absolute (instantaneous) load voltage is always lower than the supply voltage, the peak-peak load voltages in bipolar mode may exceed the single-supply level, while forcing biphasic currents. Maximum load voltage during a stimulation phase is $|V_{dd} - V_{drop}|$, where, V_{dd} is the single supply voltage and V_{drop} is the sum of voltages dropped across the current source and the forward biased diodes. Peak-peak load voltage range, while combining positive and negative phases, is therefore $2(|V_{dd} - V_{drop}|)$. Assuming, V_{dd} is 5 V and V_{drop} is 2 V, the peak-peak load voltage range has been 6 V.

Low voltage control signals (eg. 3.3 V) have been sufficient while using lower impedance electrodes (eg. < 1 KΩ). However, for larger load impedances, a digital level translator may be used with internal low voltage compatible control inputs, for microcontroller based operations.

3) Inter-Phase Delays: Inter-phase delays may be added between the stimulation phases by means of turning *OFF* the potential difference at the control nodes *T1* and *T2*. The terminals *T1* and *T2* must be either configured at equal logic level ('*0*' or '*1*') or tri-stated during inter-phase delays.

III. Bench-Top Electrical Measurements

The low overhead charge balancing stimulator has been implemented using commercially available components for demonstration of the proof-of-concept and rapid prototyping. Fig. 4 shows the printed circuit board (PCB) implementation with floating current sources REF200 (Texas Instruments Inc., TX), and Schottky diodes BAS70-04 (Diodes Inc., TX). The measurement set-up and electrical characteristics have been described below.

A. Electrical Characterization Set-Up

Fig. 5 depicts block diagram of the custom set-up used to evaluate performance of the stimulator front-end. An arbitrary function generator (Agilent Technologies Inc, CA, Model 33250A) has been used to provide control voltages and timing signals. The control signals of ± 10 V has been applied through *T1* and *T2*. The output of the stimulator has been connected to the load impedance through a current sense resistor, $\mathrm{R_s}$. Instrumentation amplifiers with wide bandwidth (8 MHz), very high input impedance (FET input) and fully differential

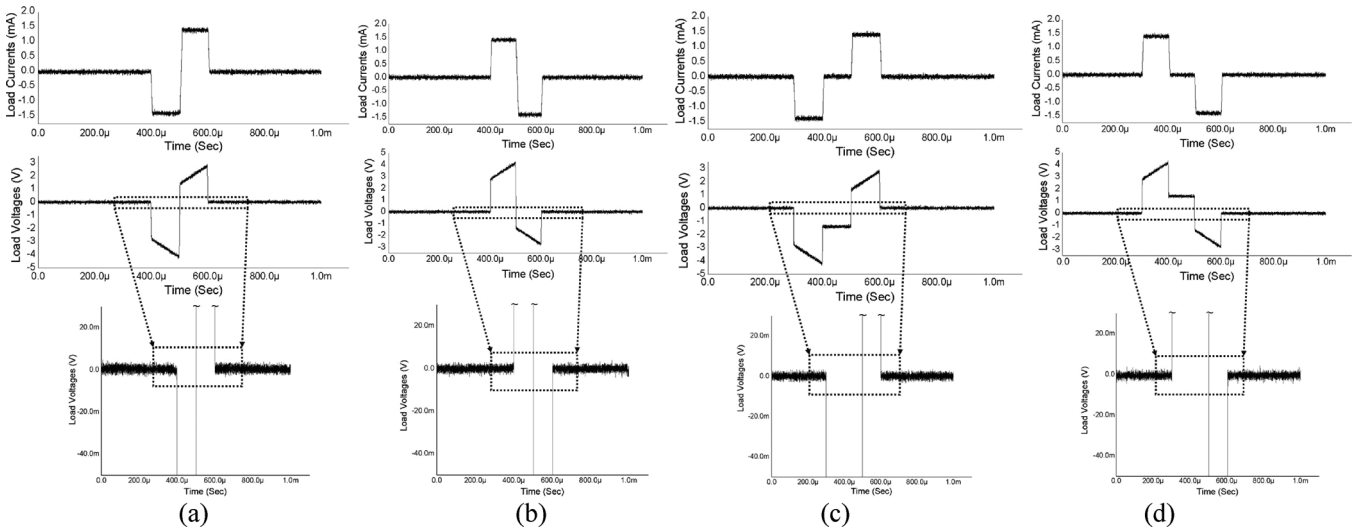

Fig. 6. Oscilloscope traces of stimulated currents and load voltages along with magnified baseline potentials,with 1.4 mA biphasic stimulationsand $2\ \mathrm{K} + 100\ \mathrm{nF}$ series RC load. (a) Cathodic-first. (b) Anodic-first. (c) Cathodic-first with interphase delay. (d) Anodic-first with inter-phase delay. The insets show the pre and post-stimulated baseline voltages across the load.

outputs have been used to accurately measure load currents (*A1*) and voltages (*A2*). The amplifier *A1*, configured with a variable gain for a suitable output voltage range and high signal-to-noise ratio, has been used to measure voltage drop across $\mathrm{R_s}$, due to stimulated currents. *A2* has been implemented with a unity gain for maximum bandwidth. The outputs of the amplifiers have been connected to a high resolution (24-bit) analog to digital converter (ADC) card (Texas Instruments Inc, TX, Model ADS1278PDK) with approximately 21 ENOBs (effective number of bits). Voltages and currents have been registered simultaneously at a 128 ksps sampling rate. A shielded enclosure (ground connected Faraday cage) has been used to reduce line noise (60 Hz). A workstation computer has been used to acquire, store and analyze data. Oscilloscope and source-meter based measurements have also been used for non-critical measurements, while bypassing the ADCs.

Discerning pico-ampere mismatches in milli-ampere currents require measurements precise to *nine* significant decimal digits. Therefore, the pico-ammeters and source meters at our disposal proved inadequate for the required characterization. Also, response time is slower in such instruments. 24-bit ADC is very useful in such precise and accurate measurements.

A variety of loads have been used to evaluate the stimulator. A series connected resistor and capacitor (RC) was used to mimic quasi-static electrode-electrolyte interface, which is a useful model to characterize the charge balancing performance [30]. Residual voltages after biphasic stimulations, using such RC load, reflect the accuracy of net charge injection. This is based on the fact that true constant current biphasic stimulation with equal phase durations is expected to charge and discharge an ideal capacitor symmetrically, with *zero* post-stimulation voltage. Charge error, if any, can be calculated by multiplying the measured residual voltage with the capacitance value ($Q_{error} = C_{load}V_{residual}$). Resistive loads are also useful to find settling time and accuracy of current magnitudes under steady states.

The average DC offset voltages and baseline noise in the data acquisition hardware have been noted at the beginning of each measurement and subtracted subsequently from acquired data. Multiple readings have been registered for all the parameters and averaging was applied for better accuracies. Post-acquisition analysis has been adopted for high precision and reliable charge error measurements.

B. Current and Voltage Waveforms

Fig. 6 shows the measured load voltage and current waveforms while passing biphasic currents of various shapes at 1.4 mA amplitudes. The electrode impedance has been mimicked by using a series connected 2 KΩ resistor (solution resistance) and low leakage 100 nF capacitor (interfacial capacitance). Anodic-first and cathodic-first, with and without inter-phase delay based waveforms have been demonstrated. The baseline load voltages have been found identical at pre- and post-stimulation instances (Fig. 6, insets). This is in contrast to any post-stimulation voltage overshoot due to charge imbalance. The load voltages are found constant (stable) during the inter phase delays due to high output impedance of the stimulator and negligible leakage (charge loss) through the load capacitor.

C. Post-Stimulation Baseline Voltage Accuracy

Insets in Fig. 6 show the oscilloscope based single cycle baseline voltages. The baseline potentials, after stimulation cycles, resume back to pre-stimulated voltages. Minute post-stimulation voltage overshoots are unobservable. However, it is interesting to know the spread of post stimulation baseline voltages, resulting after applications of tens of stimulation pulses, as in practical cases. Fig. 7 shows the statistical spread of the relative residual voltage for 1.4 mA stimulations, measured over 20 anodic-first stimulation cycles. A mean post-stimulation baseline

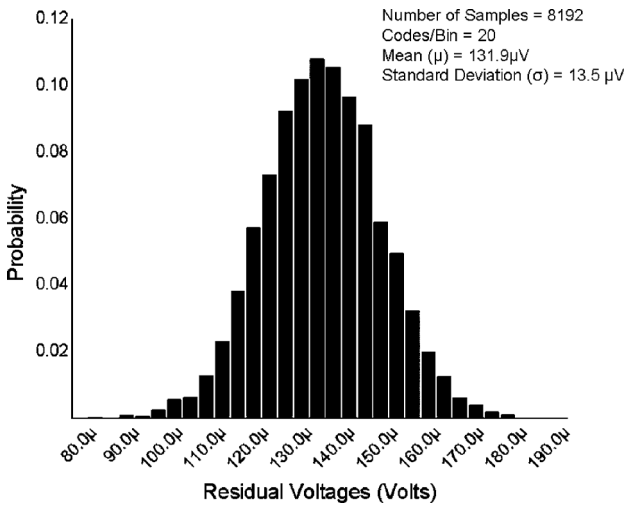

Fig. 7. Probability distribution function of the post-stimulation residual voltage with 1.4 mA, averaged over 20 cycles, measured with 24-bit data acquisition system.

voltage of 132 μV has been measured, which is same as that of the offset in the measurement set-up.

D. Current Accuracy

Current errors have been measured to gauge sourcing and sinking accuracies of the stimulator. The average of the mean values (20 readings) from the steady-state positive and negative currents' distributions have been subtracted from one another to calculate mismatches. Measured errors are less than 27 pA for 1.4 mA and 8 pA for 100 μA magnitudes.

The instantaneous load and drop-out voltages across the floating current sources vary during stimulation phases, due to capacitive nature of the load. The current supplied by the floating current source has a small variation as the voltage across it approaches the minimum specified voltage. Since the mean voltage across the load is not exactly centered (non-symmetric), these variations in the two phases will not be equal and may result in very small mismatches. This can be handled in one of the two ways: (i) use of high control voltages at *T1* and *T2*, such that it will maintain large enough voltage drop across the current source, or, (ii) application of an offset voltage at *T1* and/or *T2*, which would equalize small deviations in the two phases, such that there is no net charge imbalance.

Both the ways have been tested using the presented stimulator's front-end. ± 10 V control signal was found sufficient for lower impedance loads (eg. Up to 1.4 mA with 5 KΩ). Whereas in case of higher impedence loads, an offset of up to 1 V was useful. In monopolar mode, this was applied at V_{mid}. In Bipolar mode, the offset was applied to *T1* through a level shifter, as shown in Fig. 2.

Leakages in series connected reverse biased diodes have a miniscule effect on current imbalance. The difference in leakages through diodes fabricated in the same package and batch, during positive and negative currents, is less than 5 pA. Mismatch due to leakages through diodes may increase somewhat at higher voltages like > 10 V, but it is unlikely to be substantial. Mismatched *ON* state resistances will also have negligible impact on stimulated current accuracies.

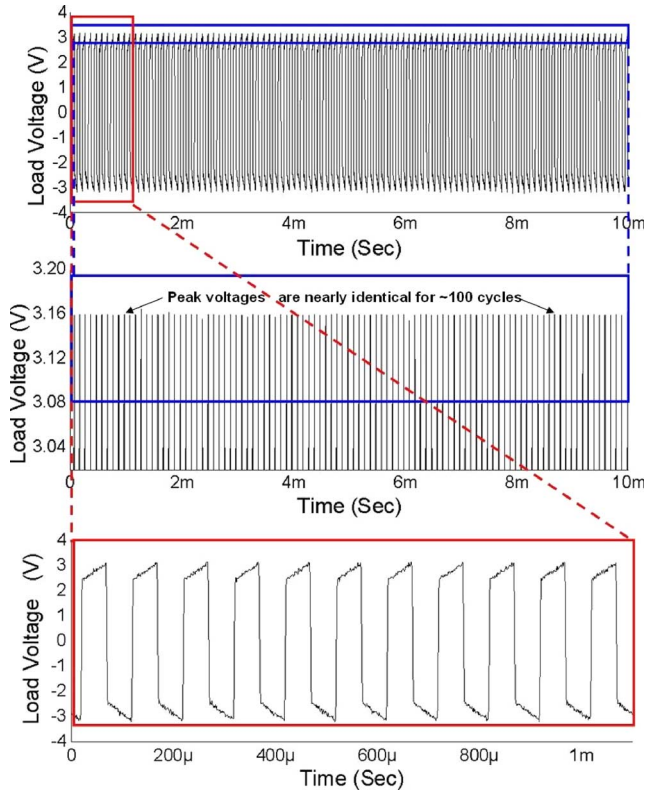

Fig. 8. Multi-cycle stimulation based charge error measurements. The upper trace shows continuous load voltages over 100 stimulations cycles at 1.4 mA. The middle trace shows the peak load voltages during such stimulations. The lower trace depicts magnified load voltages for 11 cycles.

Drifts in absolute current magnitude are unobservable within a short time span (*micro* or *milli-seconds*). Long term drifts, due to temperature variations, can alter the amount of injected charges during stimulation phases. Charge balancing is likely to remain unaffected by such drifts, because of quick succession of stimulation phases within few hundreds of *micro-second*s.

E. Charge Accuracy

Charge balancing has been achieved through high accuracy matching of positive-negative currents and phase durations. Charge errors have been measured by using the instrumentation shown in Fig. 5. The absolute residual voltage (per cycle) is too small to acquire reliably due to the presence of background noise. Measurements of the accumulation of such residual voltages are observable over several (continuous) stimulation cycles. Therefore, shifts in mean (or peak) load voltages over multiple cycles indicate average charge error per biphasic stimulation cycle.

The constant current stimulator has been tested with operations over 200 million biphasic cycles at frequencies ranging between 100 Hz and 10 KHz. The mean voltage shifts have been divided by the number of stimulation cycles (after every 1 million cycles, between two data points) and multiplied by the load capacitance, to calculate average residual charge errors.

The top trace in Fig. 8 shows the load voltage for continuous 1.4 mA stimulations over 100 continuous cycles through a series connected 2 K + 100 nF RC load. The middle trace shows the magnified peak voltages. This indicates very little peak voltage

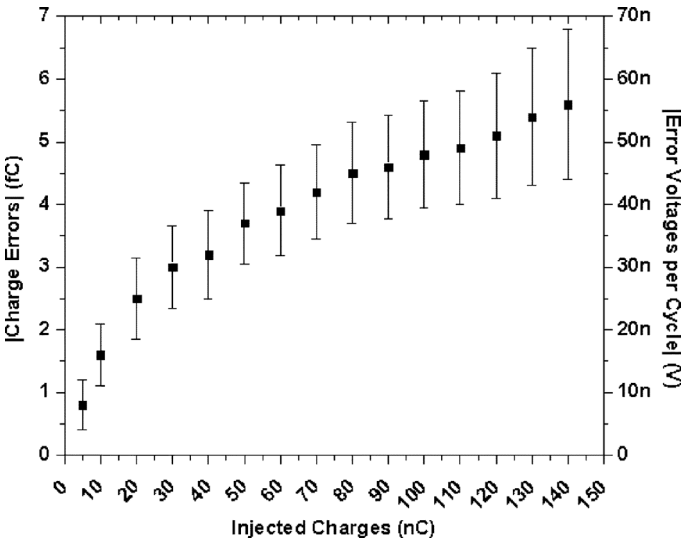

Fig. 9. Normalized charge and voltage errors along with spreads as function of injected charges per biphasic stimulation cycle.

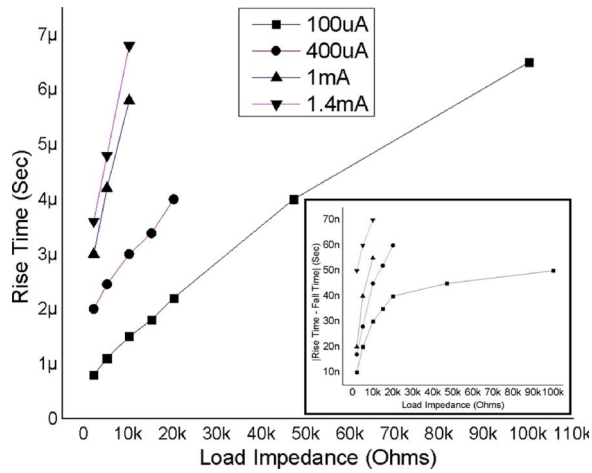

Fig. 10. Settling (rise) time as function of load impedances and stimulation currents. The inset shows the mismatch between rise and fall times.

shift due to good charge accuracy in every stimulation cycle. The bottom trace shows magnified peak-peak load voltages over 11 stimulation cycles.

Fig. 9 shows the average charge and voltage errors as function of injected charges and corresponding spreads over 20 trials, as normalized to single biphasic stimulation cycles. The errors and spreads increase with larger current magnitudes. An average baseline drift of nearly 7.5 mV (measured using 24-bit ADC) has been observed while stimulating with 100 μA and 1 million successive biphasic cycles, which accounts for 7.5 nV normalized residual voltage per cycle (calculated as 7.5 mV/1 million). Average charge mismatch per stimulation cycle has been calculated as [100 nF $\times$ 7.5 mV]/(1 million) which results in 750 aC error (150 parts per billion or ppb), for a 5 nC stimulation. Similarly, the average charge error for a 1.4 mA stimulation current, while injecting 140 nC per cycle, is close to 5.6 fC (40 ppb). The maximum spread occurs for 140 nC stimulations and comes to 1.2 fC or 12 nV (per cycle) in this case. It has also been observed that charge error does not increase linearly with current magnitudes. Offset compensation using the level shifter, as mentioned in the earlier sub-section, can even lower the charge errors, as tested in certain cases.

The calculated charge error from the measured current error has been 2.7 fC for 140 nC stimulation (1.4 mA, 100 μs/phase). Measured charge errors have been found more than the expected values due to several practical constraints. This is mainly because of increased non-symmetric leakages through the reverse biased Schottky diodes at larger voltages. Finite (very high) shunt resistance in the load capacitor contributes additional (minuscule) error in residual charge measurements. Matching of rise and fall times (temporal jitters), ambient and instrument noise are other important hurdles while performing such precision measurements in the laboratory.

F. Settling Time

Settling time depends on the combined effects of rise and fall time of control signals, turn-on and reverse recovery time of the diodes, junction capacitances in the diodes, capacitance of the floating current source and stray capacitances in PCB traces and cables. Rise time and fall time have been noted, during positive and negative cycles, while connecting resistive loads. Fig. 10 shows the rise time as functions of load impedance at selected stimulation currents. A maximum settling time of 7 μs has been observed, corresponding to load voltage transitions up to 8 V.

The inset in Fig. 10 shows the mismatch in measured rise and fall time. Rise and fall delays are closely matched in our stimulator, making it significantly advantageous at high frequency stimulations with precise charge balancing. Considering, biphasic stimulation consists of four edges (two rising and two falling), a maximum stimulation rate of 35.71 KHz can be obtained. This is higher than most practical requirements in neuronal stimulations.

G. Residual Voltages

Despite efforts to develop perfectly matched biphasic stimulators, it should be noted that even an ideally matched biphasic constant current stimulation leaves finite residual voltages at the electrode-electrolyte interface. This is due to the leaky behavior of interfacial capacitance. Charge losses occur through the charge transfer resistance (Fig. 11, lower inset), which results in residual voltage after a biphasic constant current stimulation. Fig. 11 shows the measured residual voltages while stimulating an Ag-AgCl electrode in 10 $\times$ phosphate buffered saline (PBS) with pH 7.4. Biphasic currents have been forced during 100 μs phase durations. Measured residual voltages are reasonably the identical for anodic-first and cathodic-first stimulations (Fig. 11). Small differences result due to variations in practical time instances, current magnitudes and offset in the measurement hardware. The upper inset in Fig. 11 shows the measured voltage profile at 100 μA stimulations.

Equivalent quasi-static RC circuits (electrode-electrolyte impedance) have also been stimulated using our prototype to evaluate the causes of residual voltage. Exact values (resistors and capacitor) have been measured along with rising and falling edges during the stimulations. *Spice* simulations have been performed with these measured parameters, while incorporating

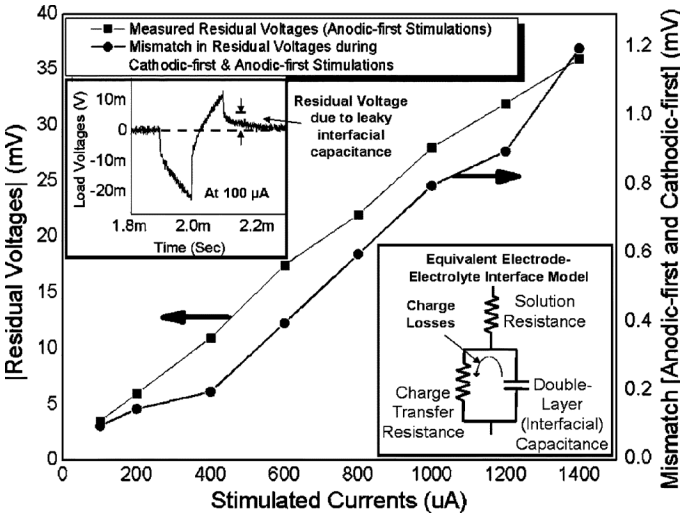

Fig. 11. Residual voltages as function of stimulated currents with Ag-AgCl electrode in saline (PBS). The upper inset shows the load voltage profile and the lower inset shows the equivalent electrode-electrolyte circuit with quasi-static loss model.

ideally matched current magnitudes and time widths. The simulation results reveal matched residual voltages as observed in practical cases, even for anodic-first and cathodic-first pulses. It has been observed that a larger charge-transfer resistance, connected in parallel to the interfacial capacitance, helps in smaller residual voltages, and vice-versa. This is due to smaller loss of charges from the interfacial capacitance through its parallel path, while getting stimulated.

Residual voltages cause stimulation artifacts, which may be nullified by means of shorting the electrodes to the reference potential. This has the drawback of adding extra charges at the biological samples due to discharging currents [28]. Hardware overhead for shorting controls and undesired feed-through noise need to be added in shorting techniques.

H. Power Consumption

The analog front-end circuit of the stimulator does not require a dedicated power supply or external bias pin, and therefore draws *zero* quiescent current. The two-terminal floating current source and the forward biased diodes dissipate little power through its time dependent VI drop, during stimulation phases only. This is similar as that of the most aggressively designed (ideal) linear current sources with no overhead circuitry and power.

The low frequency (4 KHz) operated microcontroller (MSP430F2274) based timing generator consumes 1.6 μW at 3.3 V supply, while controlling 100 Hz stimulations. The optional level shifter, used to improve the load voltage range or charge accuracy, adds up to 25 μW power. This is negligible when compared to 3.92 mW due to 1.4 mA stimulation through a 2 KΩ load. Realistic electrode impedances are generally higher which draws more power (I^2R) without additional power loss at the stimulator hardware. Table I enlists the measured electrical specifications of the analog front-end circuit of the stimulator.

TABLE I
ELECTRICAL SPECIFICATIONS OF THE STIMULATOR FRONT-END

	Parameters	Specifications
1.	Current range	100 µA to 1.4 mA
2.	Charge injection range	5 nC to 140 nC
3.	Charge error	<5.6 fC for 140 nC stimulations
4.	Stimulation frequency	Up to 31.75 KHz
5.	Input voltage range	1.5V to 40V
6.	Quiescent power	Nil (analog front-end), 25 µW (with level translator)
7.	Noise (Current)	~50pA, peak-peak
8.	Output Impedance	>100 MΩ

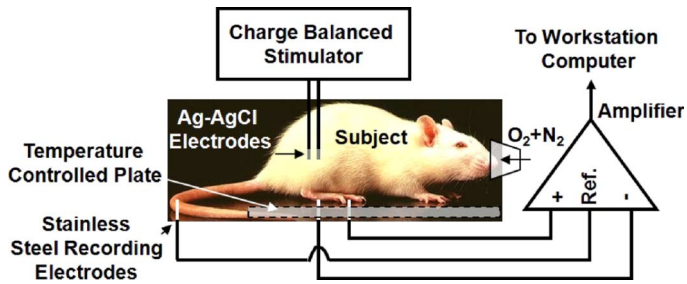

Fig. 12. *In-vivo* experimental set-up for charge balanced stimulations.

IV. IN-VIVO MEASUREMENTS

A. Experimental Arrangements

Animal trials have been performed with peripheral nerve stimulations as per the Johns Hopkins University Animal Care and Use Committee approvals. Fig. 12 illustrates the schematic of the set-up. Female Wister rats (n = 2, 250–300 g) have been placed over a temperature controlled plate and anesthetized with a mixture of 50 mg/kg of ketamine and 5 mg/kg xylazine during the experiments. Sciatic nerve corresponding to the randomly selected hind limb (left or right in each subject) was exposed at the level of femur area. A custom-made cuff electrode (0.1 mm diameter) was placed at the proximal end of the sciatic nerve. A reference wire (in bipolar mode) or button (in monopolar mode) electrode was placed inside the muscle near the distal end of sciatic nerve. Silver-silver chloride (Ag-AgCl) coated electrodes were adopted for biocompatibility and stability of electrochemical offset potentials.

Muscle evoked potentials (MEPs) were recorded using stainless steel needle electrodes from the soleus muscle. A ground electrode was placed in the tail of the subject. Commercially available 3-wire amplifier system (TDT RA16PA preamplifier and RX5 base station) was connected through an optical isolator. A standard graphical user interface (GUI) was adopted to visualize and store responses for offline analysis.

B. Closed-Loop Stimulation and Recording

The proximal end of sciatic nerve has been stimulated using the charge balanced stimulator. 100 μA to 400 μA currents were used in this experiment with 100 μs per phase durations. Continuous stream of stimulation pulses were applied through the 4 KHz operated microcontroller based driver and the analog-

TABLE II
COMPARISON OF CHARGE BALANCED STIMULATORS

	This Work	Sooksood et.al., 2010	Chun et.al., 2010	Constandinou et.al, 2008	X. Liu, 2008	Sit &Sarpeshkar, 2007	X.Fang et.al. 2007	Lee & Lam, 2007	Sivaprakasam et.al, 2005
Modes of Operation	Monopolar and bipolar	Monopolar	Bipolar	Bipolar	Monopolar	Monopolar	Monopolar	Monopolar	Monopolar
DC Current Error/ Full scale range	<27 pA/ 1.4mA	NA	1 nA/ 1 mA	3.67 µA (0.5 %)/ 735 µA	5.3 nA/ 1 mA	6 nA/ 1 mA	Voltage mode (250 pC)	2 µA/ 3 mA	7.2 µA (1.2%)/ 600 µA
Charge Error (*)	<5.6 fC for 140 nC	0.01 %	37 pC	NA	10 pC(#)	6 pC	1.25 pC (#) (0.2 %)	0.06 % (#)	14.4 pC (#)
Quiescent Power	Zero (front-end)+1.6 µW at 100 Hz (controller)	NA	10 µW	60 µW	200 µW	47 µW	50 µW	67 µW	62.5 µW (#)
Implementation Process	Discretes	Discretes	0.35 µm High voltage (simulation)	0.35 µm	1 µ SOI	0.7 µm high voltage	0.18 µm (simulation)	NA	1.5 µm

Notes: # Calculated from available data; * Expressed in equivalent units, as per available data.

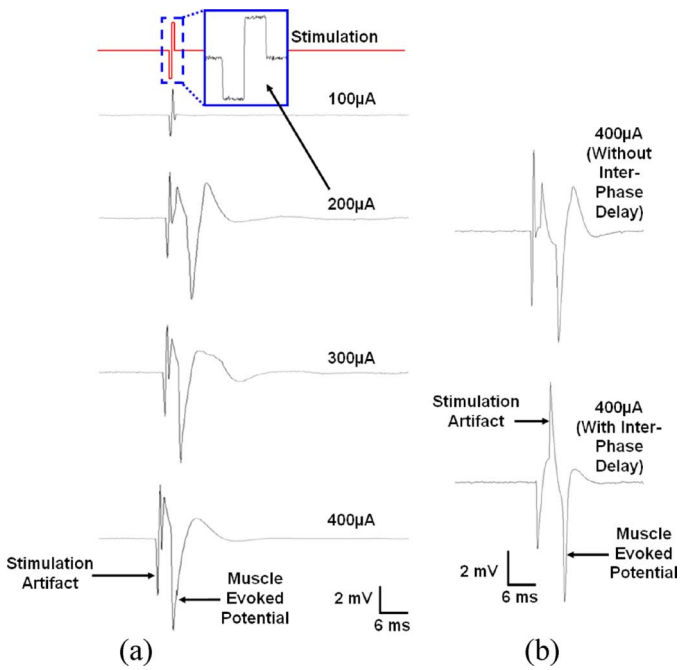

Fig. 13. Stimulation evoked responses (Muscle Evoked Potentials). (a) With bipolar stimulations. (b) With monopolar stimulations, with and without inter-phase delays.

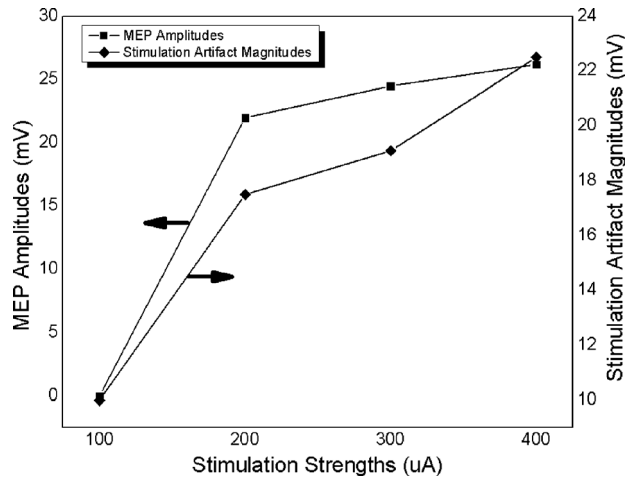

Fig. 14. Amplitudes of muscle evoked potentials (MEPs) and stimulation artifacts with stimulation strengths.

front-end. 2 Hz stimulation rate was adopted for 1 minute, followed by 2 minutes relaxation periods. This was repeated four times at each current magnitude. Stimulation strengths were varied in 100 μA steps, both for increasing and decreasing currents. Relaxation of motor neurons was allowed for 5 minutes between studies with different strengths.

Observations have been noted in three ways, namely, MEP recordings, visually observing muscle movements in the hind limb and oscilloscope based stimulation instances. An exact synchronization has been noticed in all three cases. Fig. 13 shows the stimulated charge balanced current (inset) and measured motor evoked responses in bipolar and monopolar modes of stimulation. The stimulation artifacts are visible in the recorded channel. Artifacts do not interfere temporally with the evoked responses due to use of separate stimulation-recording electrodes and optical isolation.

Fig. 14 shows the strengths of muscle evoked potentials and stimulation artifacts for applied pulses. Variations in amplitude of stimulation artifacts and evoked MEPs with stimulation strengths have been noticed. MEPs and hind limb movements were visible for currents between 200 μA and 400 μA and never for 100 μA. The threshold of stimulation thus has been 200 μA with close to 100% success rate. Thresholds are unaffected by the inter-phase delays. Larger currents than 400 μA have not been applied to avoid excessive limb movements and electrode misplacement. Injected charges have also been controlled by adjusting widths of stimulation phases at various current magnitudes.

Anodic-first stimulations exhibited relatively less limb movements than cathodic-first types for identical amounts of current. Inflammation, localized heating and damages have not been observed in both the subjects, even with continuous stimulations for two hours in each case.

V. Conclusions

Highly flexible charge balanced stimulator architecture has been presented using a single current source for both positive and negative stimulation phases. The floating current source and the steering network based front-end exhibits better than 5.6 fC charge balancing accuracy for 140 nC stimulations (40 ppb mismatch). The stimulator operates in monopolar and bipolar modes and generates anodic-first or cathodic-first biphasic pulses with optional inter-phase delays. The biphasic stimulator's front-end exhibits *zero* quiescent currents and the digital controller consumes additional 1.6 μW. Validation results have been demonstrated with RC load, *in-vitro* Ag-AgCl electrode in saline and *in-vivo* peripheral (sciatic) nerve stimulations in anesthetized rats.

Blocking capacitors, shorting of electrodes and complex feedbacks have been eliminated, while retaining high accuracy and reliability in neuronal stimulations. Table II specifies a comparison with related work. The presented architecture exhibits better than three orders of magnitude reduction of charge errors as compared to [30].

Possible shortcoming of the charge balancing stimulator, such as the PCB size, could be mitigated through on-chip fabrications in future. Although, the design of Schottky diodes will be critical, careful layout practices can solve this challenge through modified CMOS processes. Wireless powering of the stimulator is another important and feasible improvement that would be useful for chronic and fully implantable studies.

Addition of adjustable current-to-current converter can incorporate finer adjustments of stimulation currents at the expense of relatively more charge errors and power overheads. Fail-safe features [12] and an Asynchronous Interleaved Sampling (AIS) algorithm based stimulation strategy [34] may be added in future versions.

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